AND8359/D

Timing Considerations with the Dual-CAN Transceiver

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APPLICATION NOTE

Introduction and Scope

The AMIS−42700 Dual−CAN transceiver is the interface between up to two physical bus lines and the protocol controller and can be used for serial data interchange between different electronic units at more than one bus line. It's block diagram is shown in Figure 1.

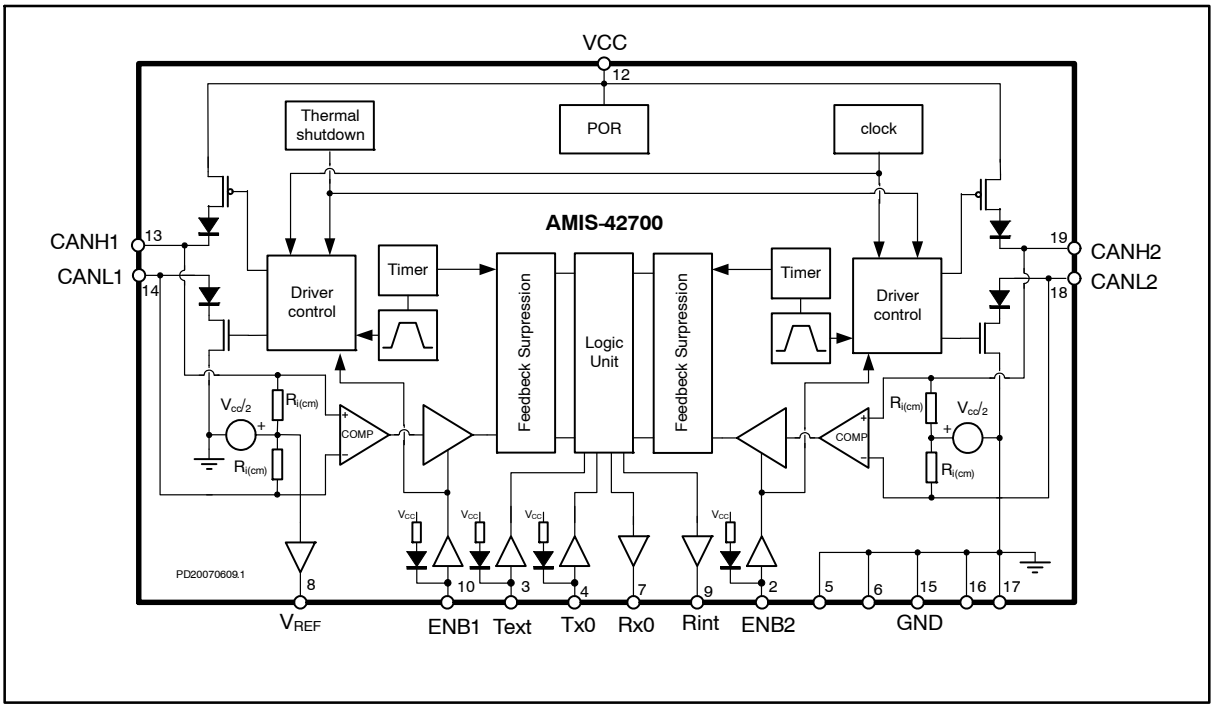

Figure 1. AMIS−42700 Block Diagram

It is able to operate in three different modes, which are presented and explained in the datasheet:

- Dual CAN
- A CAN bus extender
- A CAN bus repeater

AMIS−42700 is used in applications where the CAN communication runs simultaneously on more than 1 CAN bus and all nodes are required to take part in the same communication flow regardless on which branch they are connected. The split of the CAN bus into multiple branches in one application can be motivated by:

- The need to individually enable/disable the buses and thus modify the application topology.
- The need to isolate faulty branches (e.g. with a bus short) and thus increase the robustness of the overall system.
- The need to drive very long CAN buses (e.g. in building automation) where the voltage drop due to a non−zero cable resistance becomes non−negligible – the primary reason for the introduction of a repeater is then the recovery of the signal levels.

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As shown in the application note 1, a high−speed CAN bus topology is defined/limited mainly by:

1. The protocol timing which limits the maximum allowed length of the bus because of the signal delay.
2. The voltage levels of the bus signals, which puts limits both on the cable length and the number of nodes. The voltage drop encountered in a CAN bus line depends on the wire resistance, on the number of nodes (each of them contributing by its input impedance) and on the value of the termination resistors.

The usage of a dual−CAN transceiver allows to use more nodes and/or longer cables if they are limited by point (2) above, because the voltage levels are “restored” each time the signal passes through the dual transceiver. However, the signal is delayed by each such transition since it needs to be received and only then it can be re−transmitted. The timing limitations mentioned in point (1) above are therefore made stricter by the presence of a dual−CAN transceiver.

This application notes explains how the timing on a CAN bus is changed by the insertion of a dual−CAN transceiver and compares it with a single bus, where all nodes are directly connected to the same bus line. It will show that the allowed bus length is decreased provided that the protocol timing is the limiting factor.

SYMBOLS AND NOTATION

For the purpose of the timing calculations, the transceivers, repeaters and bus lines will be represented by simplified functional symbols and signal−flow diagrams. Only transmission and reception functionality is captured by these symbols, omitting other blocks of the components – supply, operating mode control, reference voltage outputs etc. – as they are not relevant for the considered calculations.

For a standalone CAN transceiver, these representations are shown in Figure 2. The level on pin TxD is transmitted differentially onto bus pins CANH and CANL. In return, the differential level sensed on the bus pins by the receiving part is reflected to the logical level on pin RxD. In the corresponding signal flow diagram, the total transmission delay between pin TxD and the bus level is denoted t_{dTxD}, whereas the total reception delay between the bus level and the logical value on pin RxD is denoted t_{dRxD}.

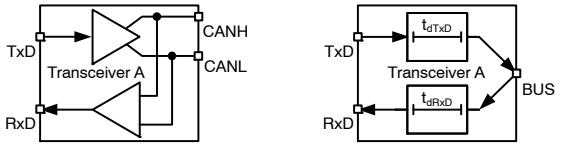

Figure 2. A standalone CAN Transceiver: The Simplified Functional Symbol and a Signal−Flow Diagram

In this application note, component AMIS−30660 will be taken as an example of a standalone transceiver. It’s delays are specified as shown in Table 1, taken from the corresponding datasheet.

Table 1. AMIS−30660 TIMING CHARACTERISTICS

$t_{d(TxD-BUSon)}$	Delay TxD to bus active	V_s = 0V	40	85	130	ns
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive	V_s = 0V	30	60	105	ns
$t_{d(BUSon-RxD)}$	Delay bus active to RxD	V_s = 0V	25	55	105	ns
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxD	V_s = 0V	65	100	135	ns
$t_{pd(rec-dom)}$	Propagation delay TxD to RxD from recessive to dominant	V_s = 0V	70		245	ns
$t_{d(dom-rec)}$	Propagation delay TxD to RxD from dominant to recessive	V_s = 0V	100		245	ns

For the calculations with the signal diagram from Figure 2 in the following sections, the sum (t_{dTxD} + t_{dRxD}) will be denoted t_{dLoop} and considered to be 245 ns, thus covering the worst case of the datasheet values.

The dual−CAN component AMIS−42700 can be depicted as shown in Figure 3 based on the same simplifications as in the case of the standalone transceiver. In addition, the logic block relating both CAN channels is not fully represented by the signal diagram as it’s not relevant for the bus−timing aspects. Instead, direct signal flows with zero delay are connecting inputs Tx0 and Text with outputs Rx0 and Rint. In reality, these links have a non−zero delay (e.g. Tx0 to Rx0 delay) and are not fully present (e.g. signal on pin Text is not directly related to pin Rint).

1. ISO11898/1 − Road vehicles − Controller area network (CAN) − Part 1: Data link layer and physical signaling

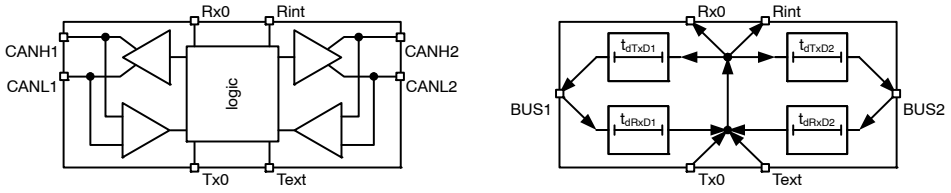

Figure 3. AMIS−42700: The Simplified Functional Symbol and a Signal−Flow Diagram

The datasheet timing parameters for transmission and reception with AMIS−42700 are shown in Table 2. Compared to the standalone transceiver AMIS−30660, the individual values are slightly different, but the sum of reception and transmission delay can be taken the same as for AMIS−30660. In the following paragraphs, the sum $t_{dLoop} = (t_{dTxDi} + t_{dRxDi})$ – symbol "i" being either 1 or 2 – will be taken as 245 ns.

Table 2. AMIS−42700 TIMING CHARACTERISTICS

$t_{d(Tx-BUSon)}$	Delay Tx0/Text to bus active		40	85	120	ns
$t_{d(Tx-BUSoff)}$	Delay Tx0/Text to bus inactive		30	60	115	ns
$t_{d(BUSon-RX)}$	Delay bus active to Rx0/Rint		25	55	115	ns
$t_{d(BUSoff-RX)}$	Delay bus inactive to Rx0/Rint		65	100	145	ns

Example A: Single CAN Bus

The first example explains how the timing criteria apply to a simple CAN bus (with only single transceivers) which is shown in Figure 4. Two arbitrary chosen nodes, denoted Node A and Node B are connected to a CAN bus, whose length between both nodes is denoted L_{line}.

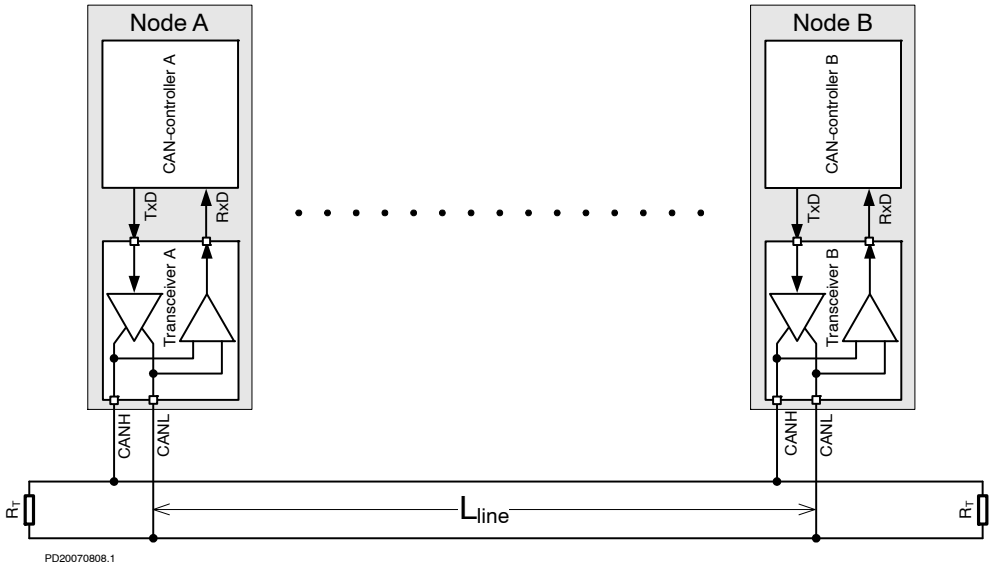

Figure 4. Simple CAN Bus Topology

For the timing calculations, each transceiver can be replaced by its corresponding signal−flow model defined in section "Symbols and Notation", while the line between both nodes is modeled as a single delay element t_{dLine}. The resulting signal−flow diagram is depicted in Figure 5. In this diagram, the delay of the CAN controllers and that of the connections between the transceivers and controllers is neglected as it's typically much lower than the delay of the transceivers and the line itself.

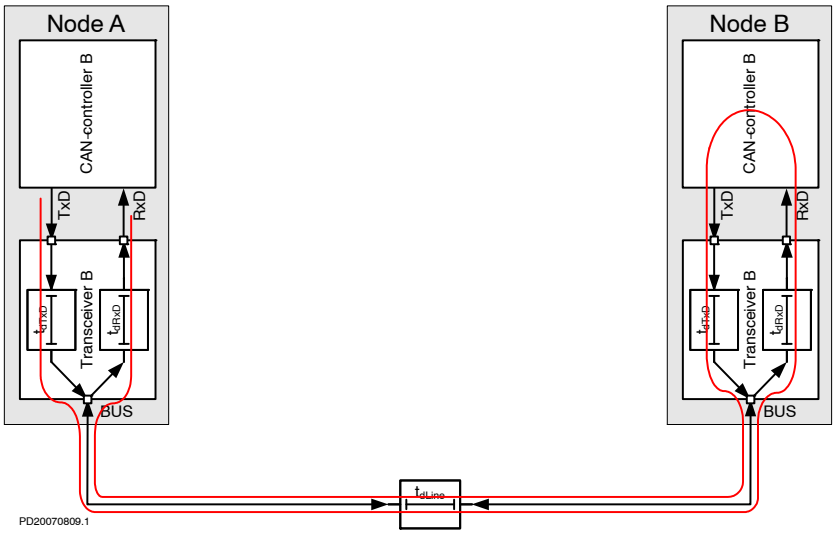

Figure 5. Signal−Flow Diagram of the Simple CAN Bus Topology

As explained in the application note 2, the overall communication delay in a CAN system is critical namely in two situations:

1. When arbitration between more nodes takes place.
2. When acknowledgement is being transmitted.

In both above cases, the overall signal propagation time from one CAN controller to any other controller and back must fit within the propagation segment of one bit time (see [1] and [2]). In the example from Figure 4, we will consider the communication to be synchronized with Node A. When arbitration or acknowledgement takes place, then signal transmitted by Node B must be correctly sampled by Node A, knowing that Node B is late compared to A because of the synchronization and, in addition, the signal must travel from B to A before it can be sampled.

Following the signal−flow in Figure 5 along the dotted line, starting at pin TxD of node A, we come to the following overall delay:

$$t_{dTOT} = t_{dTxD(A)} + t_{dLine} + t_{dRxD(B)} + t_{dLine}t_{dRxD(A)}$$

Where the first three terms account for the delay due to the synchronization of node B towards node A, and the other three terms express the propagation of a signal transmitted by node B and which is to be correctly sampled by node A. We can consider both nodes using the same transceiver, leading to the following simplification:

$$t_{dTOT} = 2 \times t_{dLine} + 2 \times \left(t_{dTxD} + t_{dRxD}\right) = 2 \times \left(t_{dLine} + t_{dLoop}\right)$$

Where t_{dLoop} denotes the sum of the transmission and reception delays of one transceiver. The line delay will be taken as proportional to the line length with the ratio of $5ns/m$ for the purpose of this application note:

$$t_{dLine} = 5\ ns.m^{-1} \times L_{line}$$

The overall delay t_{dTOT} must be inferior to the propagation segment T_{PROP_SEG} of the bit time, which results in an upper limit of the line length:

$$L_{line} \leq \frac{T_{PROP\_SEG} - 2 \cdot t_{dLoop}}{2 \times 5\ ns/m^{-1}}$$

Table 3 shows maximum bus lengths (i.e. maximum distance between any two nodes) for different bit rates and for two different timing settings of the CAN controller:

1. The propagation segment equals 15/32 of one bit time – less precise clock can be used and more time is left for the message treatment. The resulting timing limits are stricter and the bus can't communicate at 1 Mbps – the line length resulting from the timing criterion is a negative number.
2. The propagation segment equals 29/32 of one bit time – which is the best setting achievable from the point of view of the propagation delay – the allowed bus length for 1 Mbps is as high as 42m in our case. However, this timing setting requires a very precise clock for the CAN controller and very fast message treatment.

2. AND8357/D − Topology Aspects of a High−Speed CAN Bus, AMIS42000/AMIS30660 application note, 12−Oct−2006

Table 3. MAXIMUM BUS LENGTH OF A SINGLE CAN BUS AS LIMITED BY THE CAN PROTOCOL TIMING

t_{dLoop} = 245 ns t_{dLine} = 5 ns/m · L_{line}		T_{PROP_SEG} = 15/32 of bit time		T_{PROP_SEG} = 29/32 of Bit Time	
bit rate	bit time	T_{PROP_SEG} (ns)	Maximum Bus Length (m)	T_{PROP_SEG} (ns)	Maximum Bus Length (m)
1 Mbps	1 μs	469	< 0	906	42
500 kbps	2 μs	938	45	1813	132
250 kbps	4 μs	1875	139	3625	314
125 kbps	8 μs	3750	326	7250	676

It shall be noted, that for the lower bit rates, the resulting line length might not be allowed because of the voltage drop criteria, which depend on the total number of nodes, on the wire resistance and on the precise value of the termination resistor.

Example B: Repeater/Dual−CAN Configuration (Two CAN Buses Connected with AMIS42700)

The principle schematics of AMIS−42700 used in its repeater/dual−CAN configuration is shown in Figure 6. The main difference of a dual−CAN bus configuration compared to a bus repeater is the possibility to disable both buses individually and the possibility to use AMIS−42700 itself as one of the nodes by connecting a CAN controller to its digital interface. For the purpose of this application note, these features are not relevant – the communication between AMIS−42700 and any other node has the same timing aspects as the communication between any two nodes connected on the same bus branch. The resulting timing limitations are identical with the single CAN−bus example above.

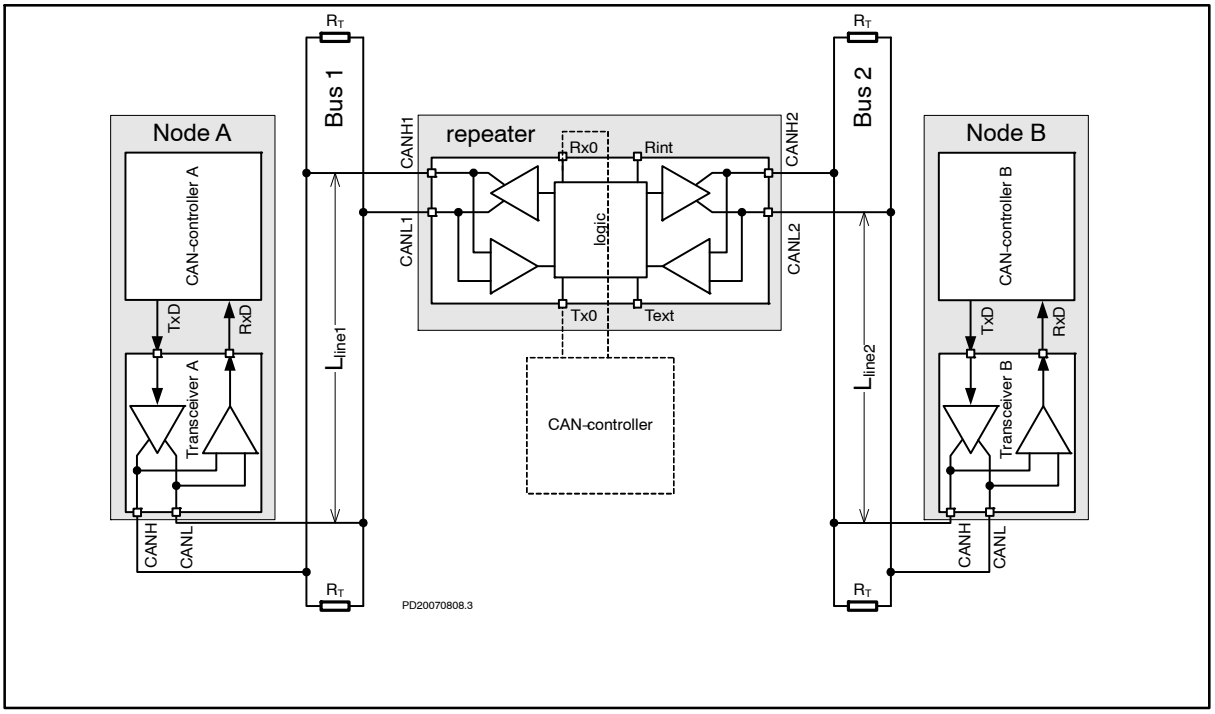

Figure 6. Example of AMIS42700 in the Repeater/Dual−CAN Configuration

Therefore only the communication between two nodes connected on different bus branches will be analyzed with the help of the signal diagram in Figure 7, where only the relevant signal path between Node A and Node B is shown.

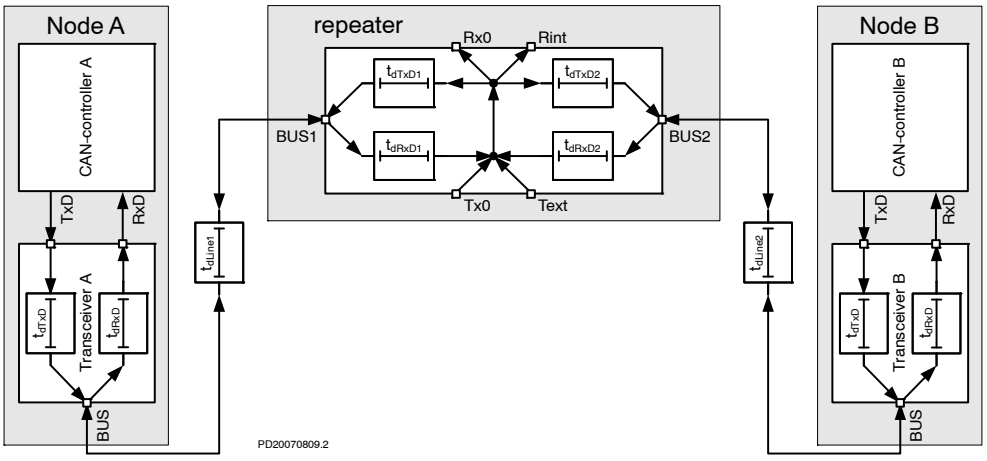

Figure 7. Partial Signal−flow Diagram of the Repeater/Dual−CAN Configuration

Similarly to the single CAN−bus analysis, the total signal delay between the CAN controllers of Node A and Node B will be assessed, supposing that Node B is synchronized to Node A and either arbitration or acknowledgement takes place. Then the total signal delay t_{dTOT} will be:

$$t_{dTOT} = t_{dTxD(A)} + t_{dLine1} + t_{dRxD1(r)} + t_{dTxD2(r)} + t_{dLine2} + t_{dRxD(B)} + t_{dTxD(B)} + t_{dLine2} + t_{dRxD2(r)} + t_{dTxD1(r)} + t_{dLine1} + t_{dRxD(A)}$$

As shown in section “Symbol and Notation”, the sum of the reception and transmission delays is the same for both considered components: −AMIS−30660 and AMIS−42700 – and can be denoted by common symbol t_{dLoop}. Taking, at the same time, $L_{lineTOT}$ as the sum of both bus lengths in the above formula, and taking the same unit line delay (5 ns/m), we obtain the following criterion for the bus length:

$$LlineTOT \leq \frac{T_{PROP\_SEG} - 4 \cdot t_{dLoop}}{2 \times 5\ ns.m^{-1}}$$

Compared to the single CAN−bus example, introduction of the repeater adds more delay due to the necessity to receive and retransmit the signal in order to keep both buses logically inter−connected. The resulting allowed bus length summarized in Table 4 are shorter than in the case of a single CAN−bus. Communication at 1 Mbps is not achievable even with the propagation segment set to 29/32 of a bit time.

Table 4. MAXIMUM BUS LENGTH OF A REPEATER CONFIGURATION AS LIMITED BY THE CAN PROTOCOL TIMING

t_{dLoop} = 245 ns $t_{dLine}TOT$ = 5 ns/m · $L_{line}TOT$		T_{PROP_SEG} = 15/32 of Bit Time		T_{PROP_SEG} = 29/32 of Bit Time	
Bit Rate	**Bit Time**	**T_{PROP_SEG} (ns)**	**Maximum Bus Length (m)**	**T_{PROP_SEG} (ns)**	**Maximum Bus Length (m)**
1 Mbps	1 μs	469	< 0	906	< 0
500 kbps	2 μs	938	< 0	1813	83
250 kbps	4 μs	1875	90	3625	265
125 kbps	8 μs	3750	277	7250	627

It must be taken into account that the calculated values represent the total length of both bus segments between any two nodes connected to different branches.

As stated at the beginning of the example, the communication between the nodes on the same bus or between the repeater itself and any node remains limited as in the case of a single bus. For example, the bit rate of 1 Mbps is not possible between node A and node B in Figure 6, but could be still used when communicating on bus 1 only (or, similarly, on bus 2 only). However, the standard protocol requires that ANY two nodes on the full bus system can enter into correct arbitration or acknowledgement. Therefore the most strict of all resulting timing limits must be respected, unless a special application−specific measure is taken.

Example C: Extender Configuration (Four Buses Connected via Two AMIS42700 Chips)

The extender configuration of a CAN−bus system with AMIS−42700 is shown in Figure 8. On each of the four interconnected buses, the same timing criteria as in the case of a single bus apply. Also the communication between bus 1 and bus 2, as well as the communication between bus 3 and bus 4 were covered by the repeater/dual−CAN configuration example. Therefore the only considered case in this example will be the communication between bus 1 and bus 4 (an analogical case would be the communication between bus 2 and bus 3) when the signal passes through two AMIS−42700 components. Therefore only one node (Node A) on bus 1 and one node (Node B) on bus 4 are shown.

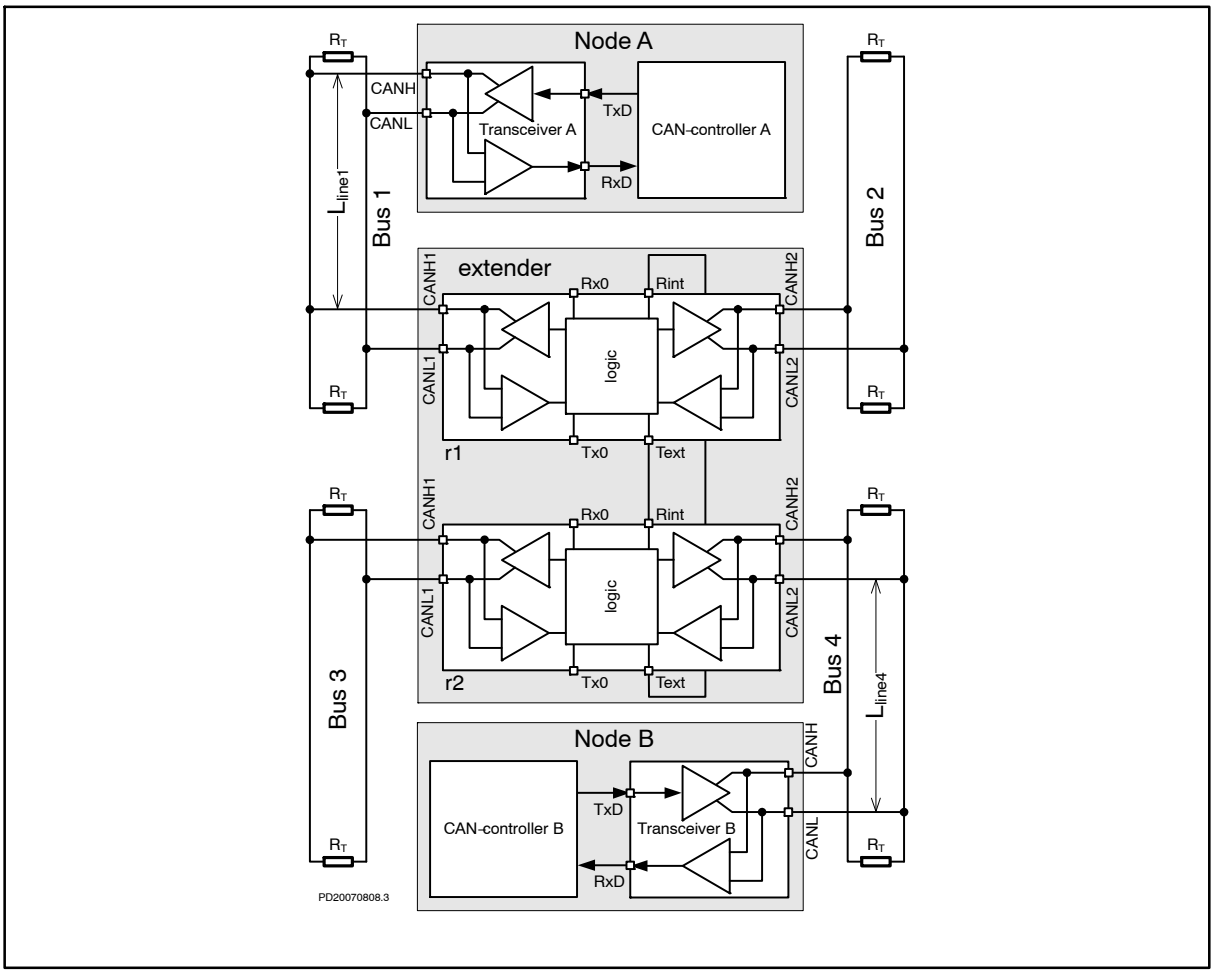

Figure 8. Example of AMIS42700 in the Extender Configuration

The corresponding signal−flow diagram is depicted in Figure 9. If Node B is synchronized to Node A and arbitration or acknowledgement takes place, the total signal delay between both nodes is:

$$t_{dTOT} = t_{dTxD(A)} + t_{dLine1} + t_{dRxD1(r1)} + t_{dTxD2(r2)} + t_{dLine4} + t_{dRxD(B)} + t_{dTxD(B)} + t_{dLine4} + t_{dRxD2(r2)} + t_{dTxD1(r1)} + t_{dLine1} + t_{dRxD(A)}$$

Using the same notation as in the previous examples, the following criterion for the total bus length between Node A and Node B results:

$$L_{lineTOT} \leq \frac{T_{PROP\_SEG} - 4 \cdot t_{dLoop}}{2 \times 5\ ns.m^{-1}}$$

Which is identical with the repeater/dual−CAN configuration.

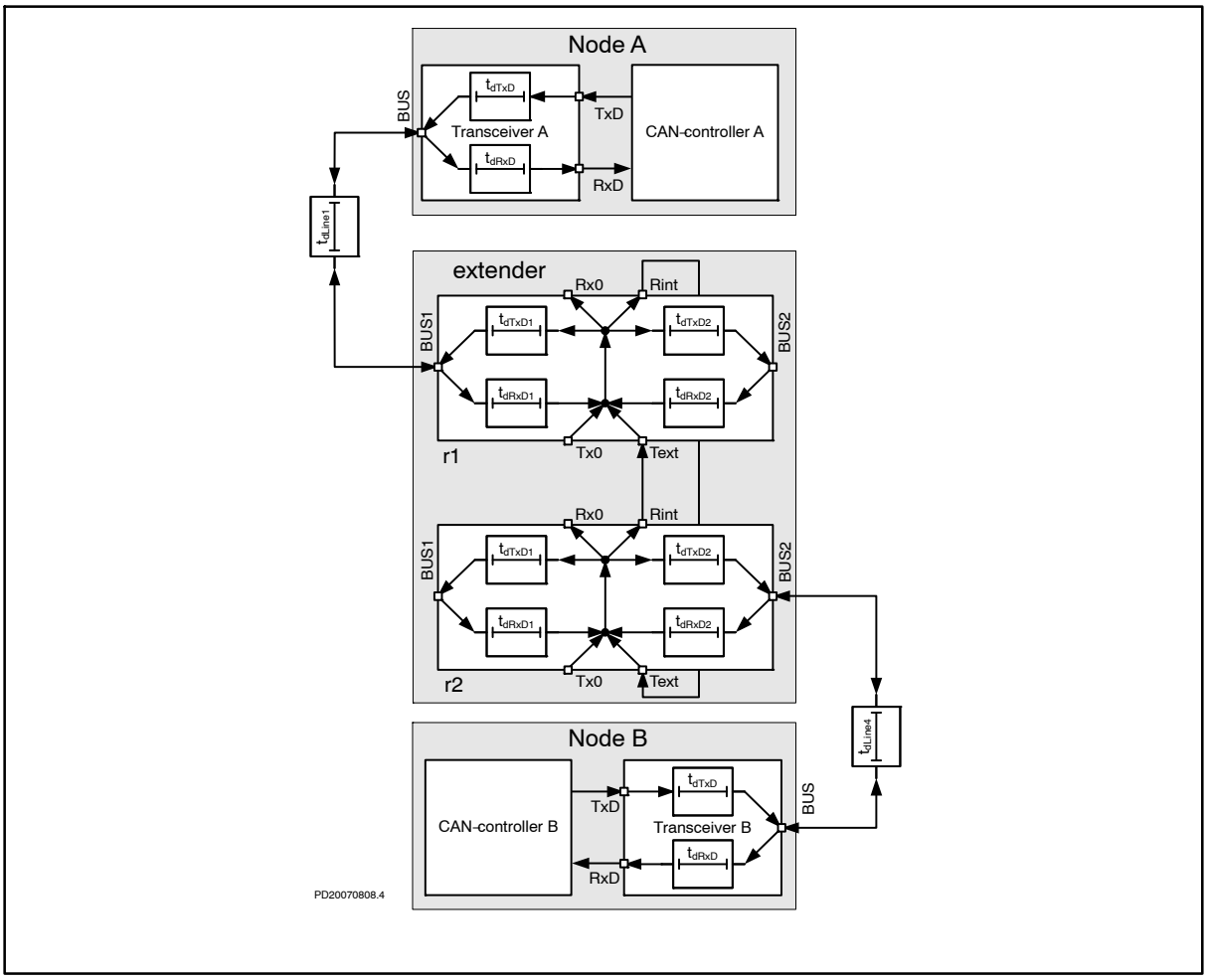

Figure 9. Partial Signal−flow Diagram of the Extender Configuration

The timing limitations in the extender configuration are thus identical to the repeater/dual−CAN configuration and numerical examples can be found in Example B. Identical results are obtained because no extra delays are considered when more AMIS−42700 components are connected. In some application−specific cases, this might be a too simplified approach, especially when additional components are included in the logical paths between two (or more) AMIS−42700 chips. This might be, for example. external logical gates or opto−couplers. If their delay is not negligible, it must be added to the total delay t_{dTOT}.

Conclusions

This application note has shown with examples of different bus topologies, that the introduction of an AMIS−42700 dual−CAN transceiver has an important influence on the timing considerations in the full CAN−bus system. Although favorable from many other points of view explained in the section “Introductory and Scope” – flexible CAN topology, increased fault−tolerance and improved signal integrity through long lines – the presence of a dual−CAN transceiver in general narrows down the timing criteria resulting from the CAN−protocol requirements set forth in [1].

As a practical consequence, it is not possible to achieve the maximum high−speed CAN bit rate (1 Mbps, see the results in Table 4) if the communication messages are supposed to pass via the dual−CAN component. This can be bypassed either by decreasing the communication speed or by implementing additional application−specific measures in the protocol or the topology itself (e.g. ensuring that only some combinations of nodes can enter into arbitration or acknowledgement process, and placing these nodes on the same bus branches). These interventions would be, however, difficult to accept as they would require special hardware and/or software implementations compared to the fully standard CAN bus systems.

References

1. ISO11898/1 − Road vehicles – Controller area network (CAN) – Part 1: Data link layer and physical signaling
2. AND8357/D − Topology Aspects of a High−Speed CAN Bus, AMIS42000/AMIS30660 application note, 12−Oct−2006

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